500.36414CX1

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicants: S. MITA, et al

Serial No.: Not yet assigned

Filed: November 13, 2001

For: PARTIAL RESPONSE DEMODULATING METHOD AND APPARATUS USING THE SAME

Group: 2634

Examiner: B. Deppe

**PRELIMINARY AMENDMENT**

Assistant Commissioner for Patents
Washington, D.C. 20231

November 13, 2001

Sir:

The following amendments and remarks are respectfully submitted prior to the Rule 53(b) Continuation Application filed on even date.

**IN THE SPECIFICATION**

Please insert before the first line of the specification the following:

-- This is a continuation of application Serial No. 09/124,840, filed July 30, 1998. --

**IN THE CLAIMS**

Please cancel claims 1-16 without prejudice or disclaimer of the subject matter thereof.

Please add new claims 17-30 as follows:

-- 17. A signal processing circuit comprising:

an equalizer for equalizing an input signal based on partial response characteristics having $(1 - D^2)$;

a discrete filter for converting the output from said equalizer into a waveform of $(1 - D^2)(c_0 + c_1D + \ldots + c_nD^n)$; and

a maximum-likelihood-demodulator for demodulating data output from said discrete filter.

18. A signal processing circuit according to claim 17, wherein the output waveform of said discrete filter is $(1 - D^2)(c_0 + c_1D + c_2D^2)$, and the coefficients $(c_0, c_1, c_2)$ are (3, 2, 1) respectively.

19. A signal processing circuit according to claim 17, wherein the output waveform of said discrete filter is $(1 - D^2)(c_0 + c_1D + c_2D^2)$, and the coefficients $(c_0, c_1, c_2)$ are (5, 4, 2) respectively.

20. A signal processing circuit according to claim 17, wherein the output wave form of said discrete filter is $(1 - D^2)(c_0 + c_1D + c_2D^2)$, and the coefficients $(c_0, c_1, c_2)$ are (2, 2, 1) respectively.

21. A signal processing circuit according to claim 17, wherein the output wave form of said discrete filter is $(1 - D^2)(c_0 + c_1D + c_2D^2 + c_3D^3)$, and the coefficients ($c_0$, $c_1$, $c_2$, $c_3$) are (2, 5, 3, 2) respectively.

22. A signal processing circuit according to claim 17, wherein the output wave form of said discrete filter is $(1 - D^2)(c_0, + c_1D + c_2D^2 + c_3D^3)$, and the coefficients ($c_0$, $c_1$, $c_2$, $c_3$) are (2, 4, 2, 1) respectively.

23. A signal processing circuit comprising:

a discrete filter for converting an input signal into an asymmetrical response, and

a maximum-likelihood-demodulator for demodulating output from said discrete filter based on said asymmetrical response.

24. A signal processing circuit according to claim 23, wherein said asymmetrical response is selected so as that data modulated by said maximum-likelihood-demodulator contains a specific error.

25. A signal processing circuit according to claim 23, further comprising:

a register for setting coefficients of said asymmetrical response.

26. A signal processing circuit according to claim 23, wherein the output from said maximum-likelihood-demodulator is directly outputted externally.

27. A signal processing circuit comprising:

an equalizer for equalizing an input signal into a symmetrical response;

a discrete filter for converting the output from said equalizer into an asymmetrical response; and

a maximum-likelihood-demodulator for demodulating output from said discrete filter based on said asymmetrical response.

28. A signal processing circuit according to claim 27, wherein said discrete filter converts so that a data response outputted from said equalizer satisfies a minimum phase transitional condition.

29. A signal processing circuit according to claim 27, further comprising:

an error corrector for correcting at least one bit error among demodulated data output from said maximum-likelihood-demodulator.

30. A signal processing circuit according to claim 27, further comprising:

an error corrector for correcting at least continuous three bits error among demodulated data output from said maximum-likelihood-demodulator. --

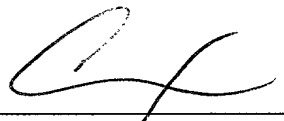
## REMARKS

Entry of the above amendments prior to examination is respectfully requested.

Please charge any shortage in fees due in connection with the filing of this paper, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (500.36414CX1).

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



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